In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Previously Presented) A method of generating energy profiles for a specific task in a processing device executing multiple tasks, comprising the steps of:

receiving a first task identifier indicative of an active task in a processing component;

receiving hardware activity signals each indicative of a hardware event in the processing device;

storing a second task identifier indicating a task to be monitored;

comparing the first and second task identifiers and generating a predetermined signal if the first and second task identifiers match;

measuring activity corresponding to the task to be monitored by counting hardware activity signals received during generation of said predetermined signal.

2 and 3. (Canceled)

4. (Previously Presented) The method of claim 1 further comprising:

periodically updating with a period T an energy profile responsive to said measuring step during operation of said processing device.

5. (Original) The method of claim 4 and further comprising the step of executing a plurality of tasks in accordance with a scenario defining scheduling of said plurality of tasks and

modifying said scenario responsive to said step of updating an energy profile.

6. (Original) The method of claim 1 and further comprising the step of performing a debugging operation responsive to said measuring step.

7. (Previously Presented) A processing device for multitasking multiple tasks comprising:

circuitry for receiving a first task identifier selected from among a plurality of possible task identifiers indicative of an active task in a processing component;

circuitry for receiving hardware activity signals each indicative of a hardware event in the processing device;

a memory for storing a plurality of second task identifier, each second task identifier corresponding to a task to be monitored;

a comparator for comparing the first and second task identifiers and generating a predetermined second task identifier match signal if the first task identifier matches a corresponding one of said second task identifiers;

a plurality of counters, each counter corresponding to one of said stored plurality of second task identifiers, each counter enabled to count said hardware activity signals when said comparator generates a corresponding predetermined second task identifier match signal.

8 and 9. (Canceled)

10. (Previously Presented) The processing device of claim 7 wherein:

said processing device is operable to periodically update with a period T an energy profile from counts of said plurality of counters during operation of said processing device.

11. (Original) The processing device of claim 10 wherein said plurality of tasks are executed in accordance with a scenario defining scheduling of said plurality of tasks and said scenario is updated responsive to said step of updating an energy profile.

12. (Previously Presented) The processing device of claim 7 and further comprising circuitry for implementing a debugging operation responsive to values in said plurality of counters.

13. (Canceled)

14. (Previously Presented) The method of claim 1 wherein:

said hardware event in the processing device includes a cache miss.

15. (Previously Presented) The method of claim 1 wherein:

said hardware event in the processing device includes a translation lookaside buffer miss.

16. (Previously Presented) The method of claim 1 wherein:

said hardware event in the processing device includes a non-cacheable memory access.

17. (Previously Presented) The method of claim 1 wherein:

said hardware event in the processing device includes a wait time.

18. (Previously Presented) The method of claim 1 wherein:

said hardware event in the processing device includes a read/write requests for a predetermined resource.

19. (Previously Presented) The method of claim 4 wherein:

said period T corresponds to a thermal time constant of the processing device.

20. (Previously Presented) The processing device of claim 7 wherein:

said hardware event in the processing device includes a cache miss.

21. (Previously Presented) The processing device of claim 7 wherein:

said hardware event in the processing device includes a translation lookaside buffer miss.

22. (Previously Presented) The processing device of claim 7 wherein:

said hardware event in the processing device includes a non-cacheable memory access.

23. (Previously Presented) The processing device of claim 7 wherein:

said hardware event in the processing device includes a wait time.

24. (Previously Presented) The processing device of claim 7 wherein:

said hardware event in the processing device includes a read/write requests for a predetermined resource.

25. (Previously Presented) The processing device of claim 10 wherein:

said period T corresponds to a thermal time constant of the processing device.